

FIG. 1

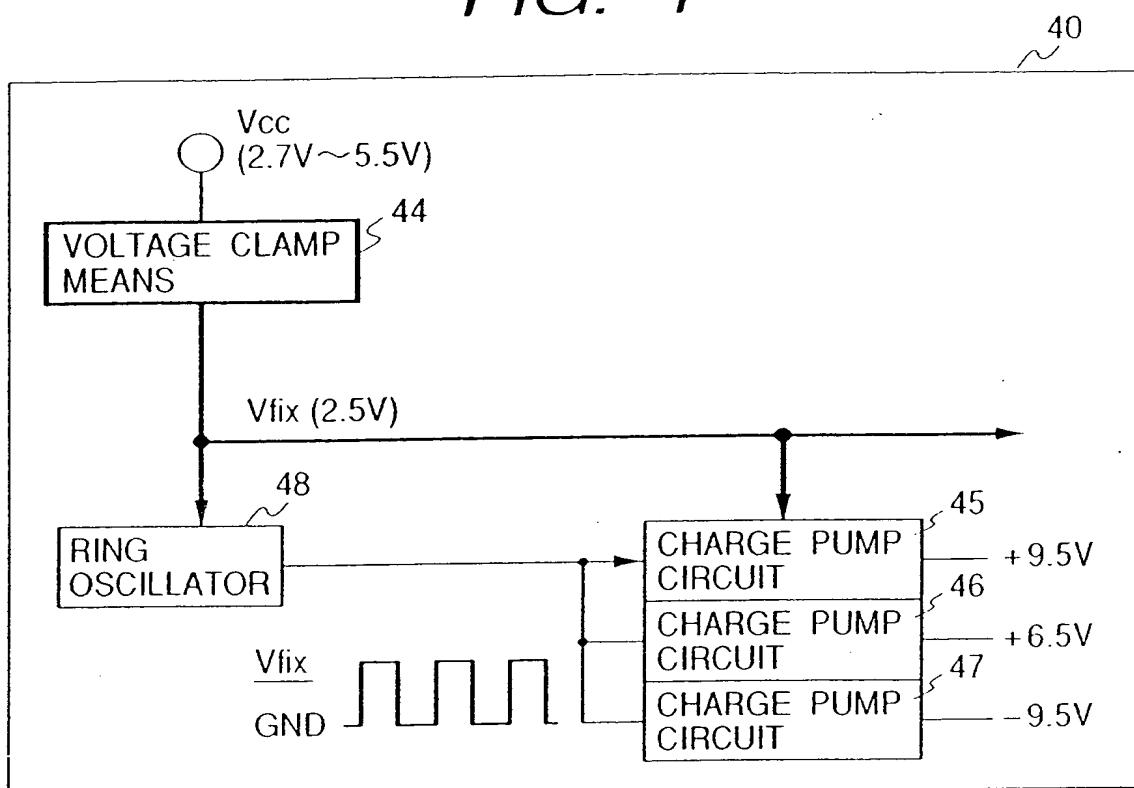
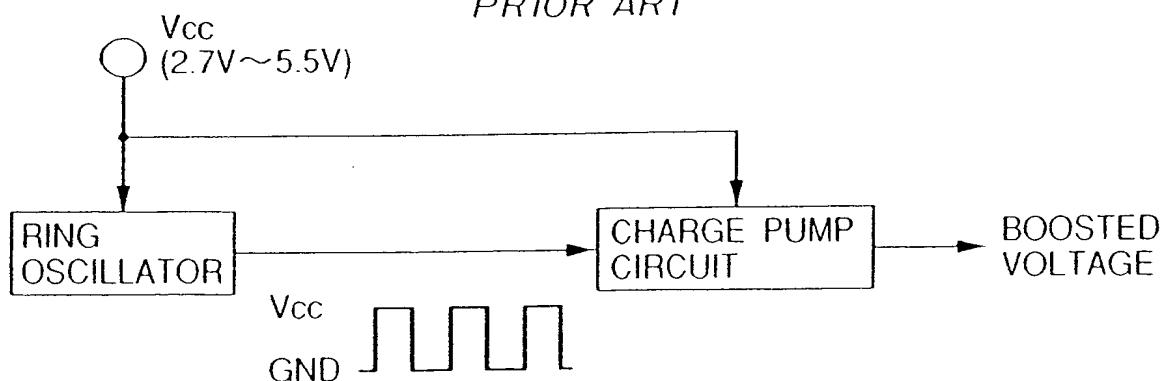
FIG. 2
PRIOR ART

FIG. 3

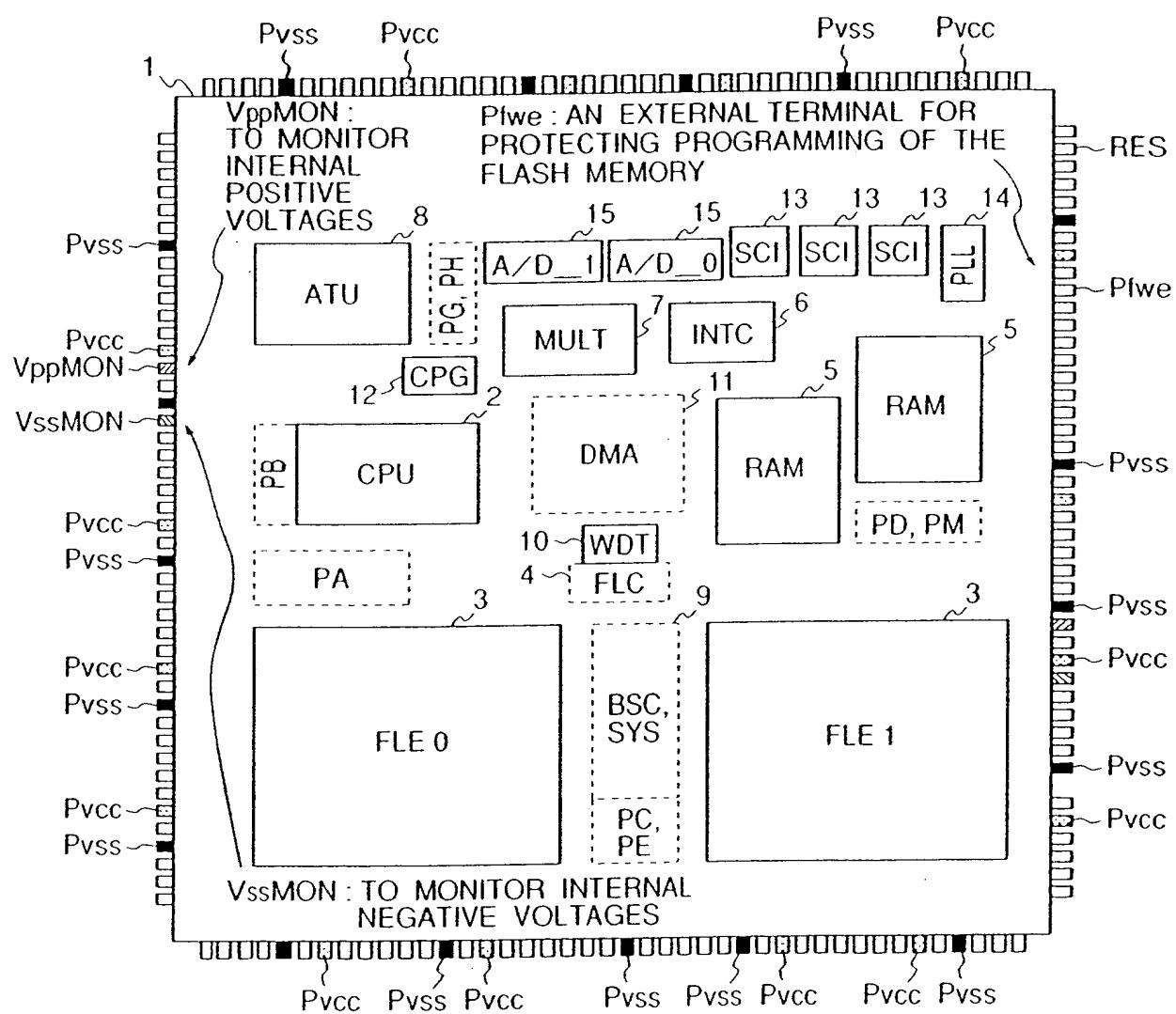
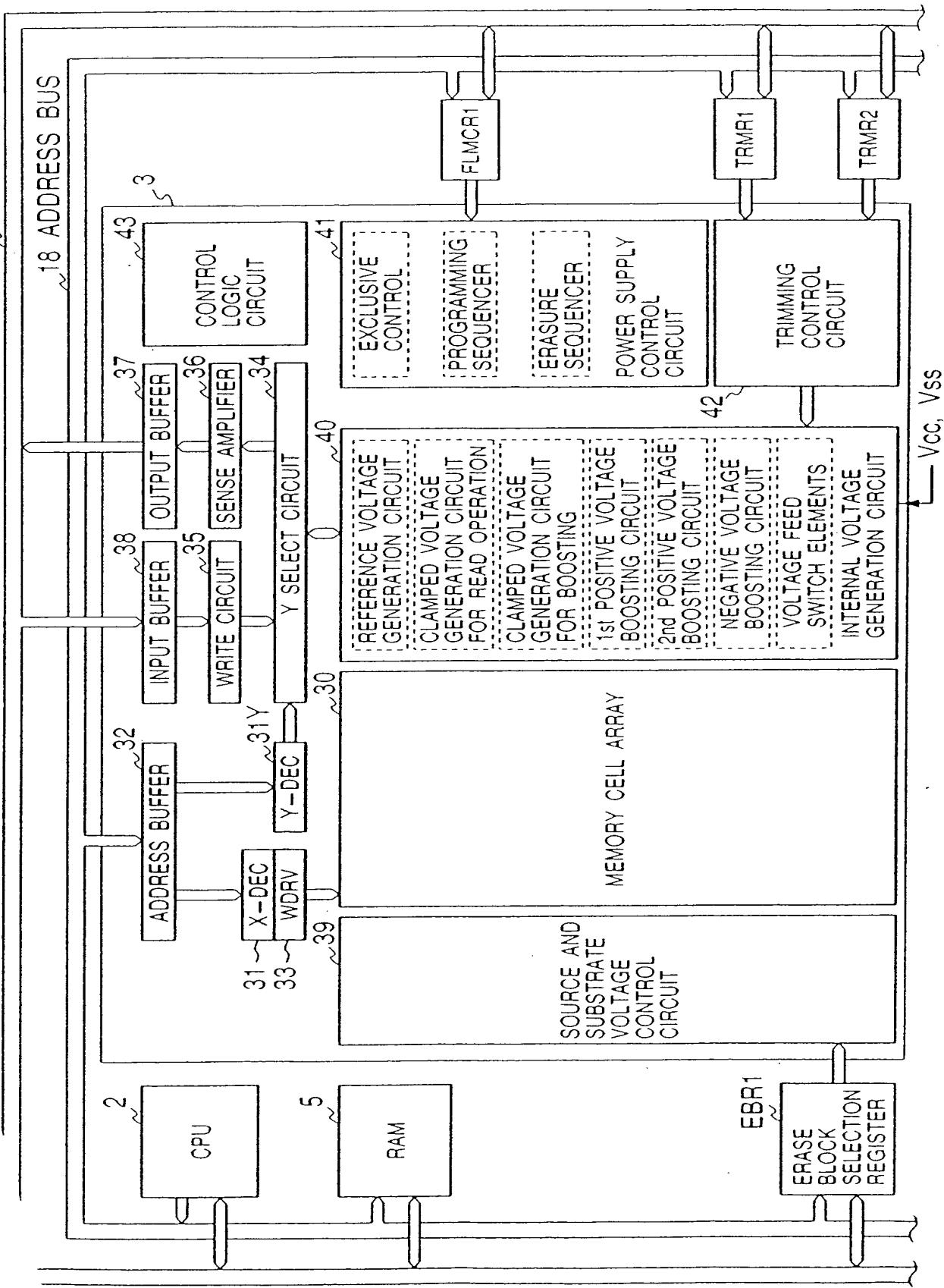


FIG. 4

17 DATA BUS

18 ADDRESS BUS

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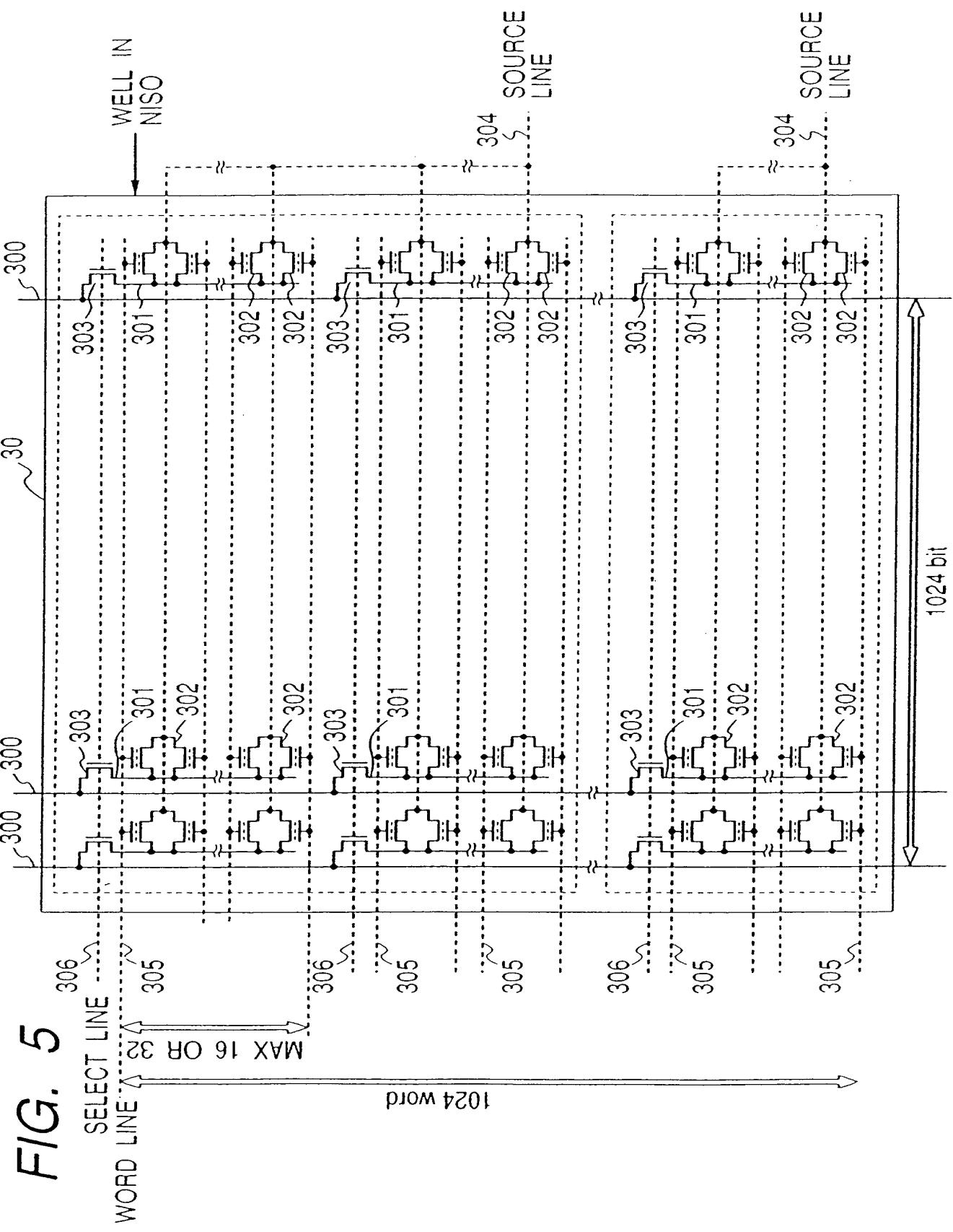


FIG. 6 (ERASURE STATE)

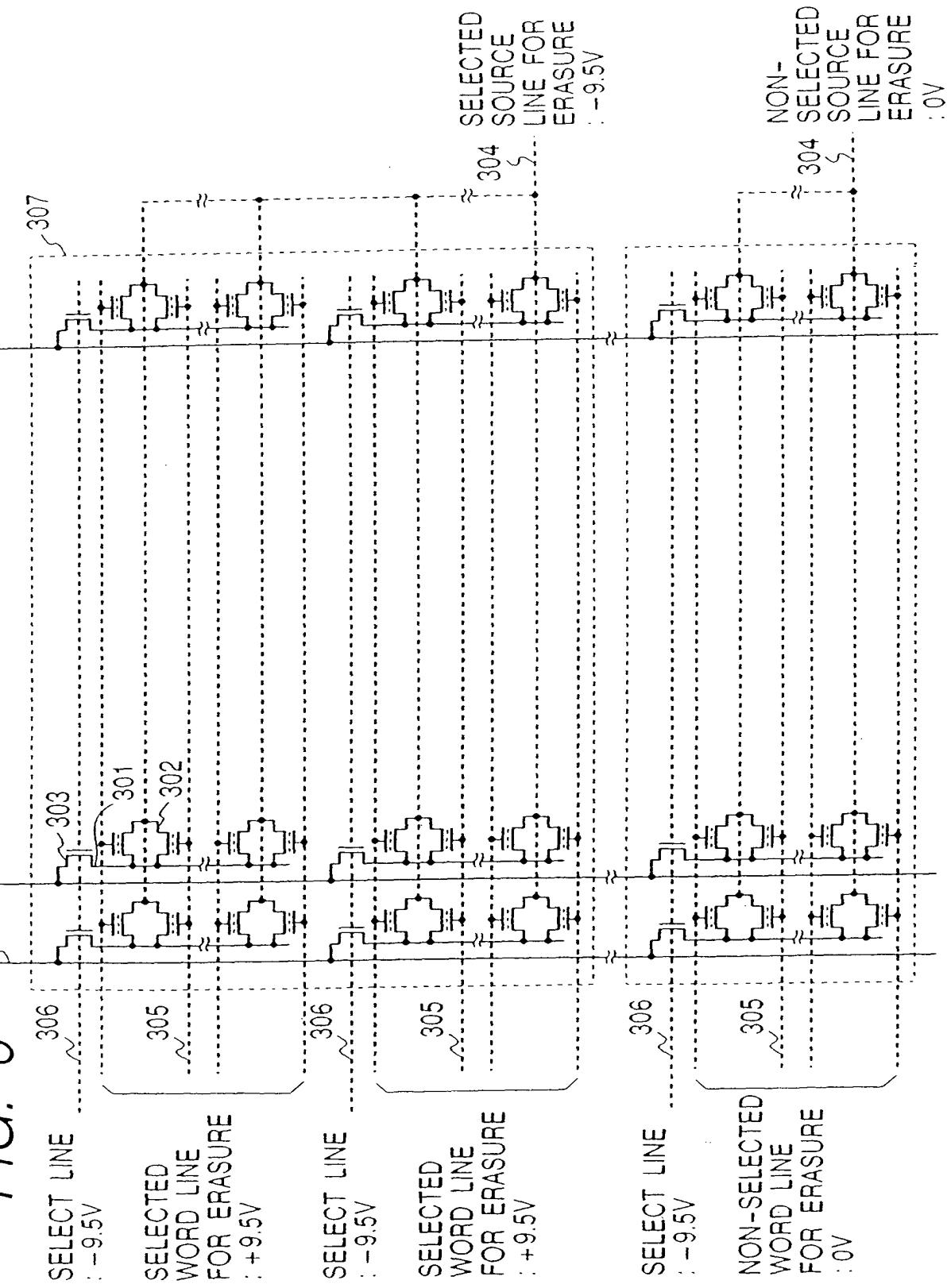


FIG. 7

(PROGRAMMING STATE)

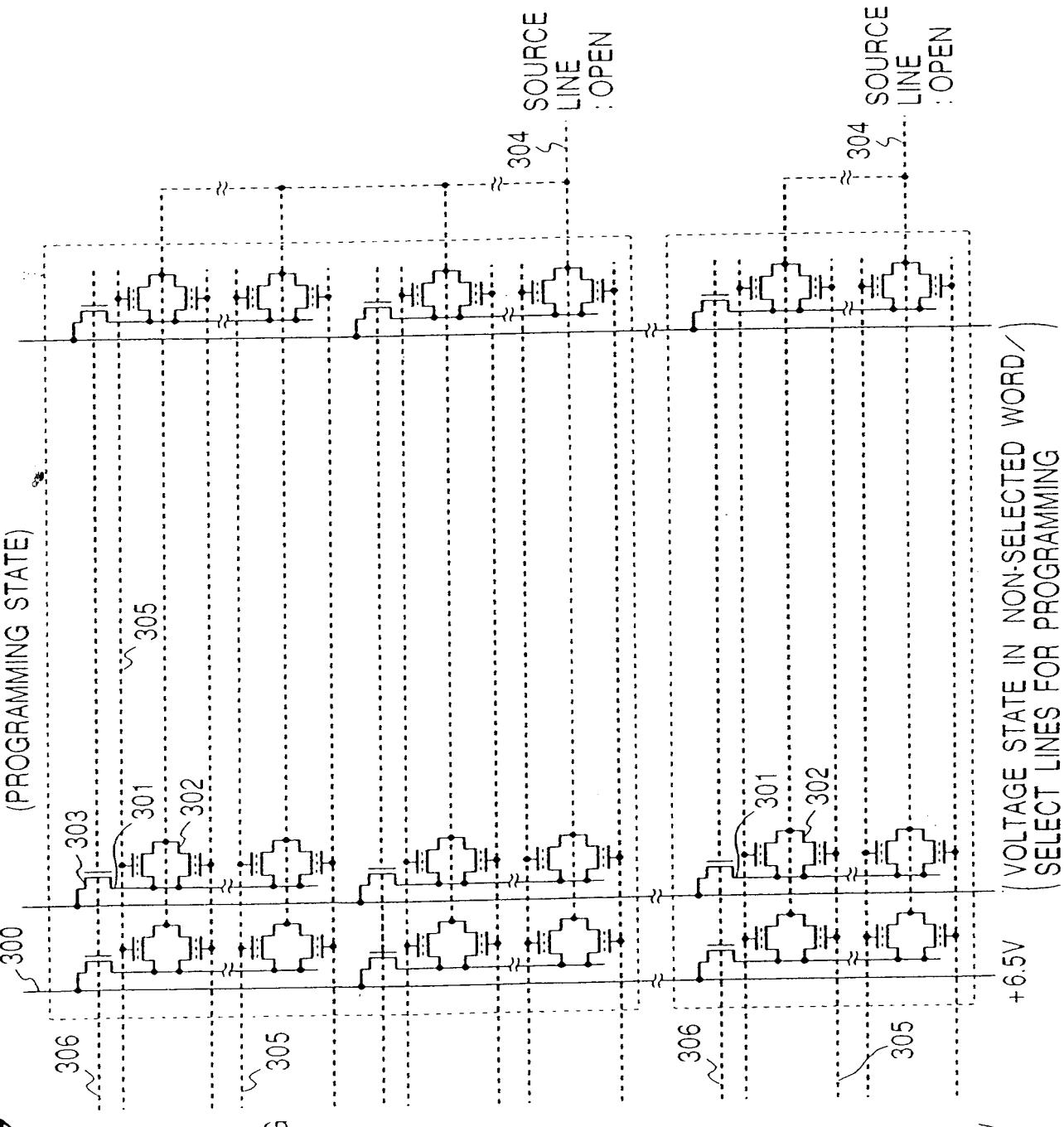
SELECT LINE
+ 9.5V

SELECTED
WORD LINE
FOR
PROGRAMMING
- 9.5V

(PROGRAMMING STATE)

SELECT LINE
+ 9.5V

SELECTED
WORD LINE
FOR
PROGRAMMING
- 9.5V



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FIG. 8

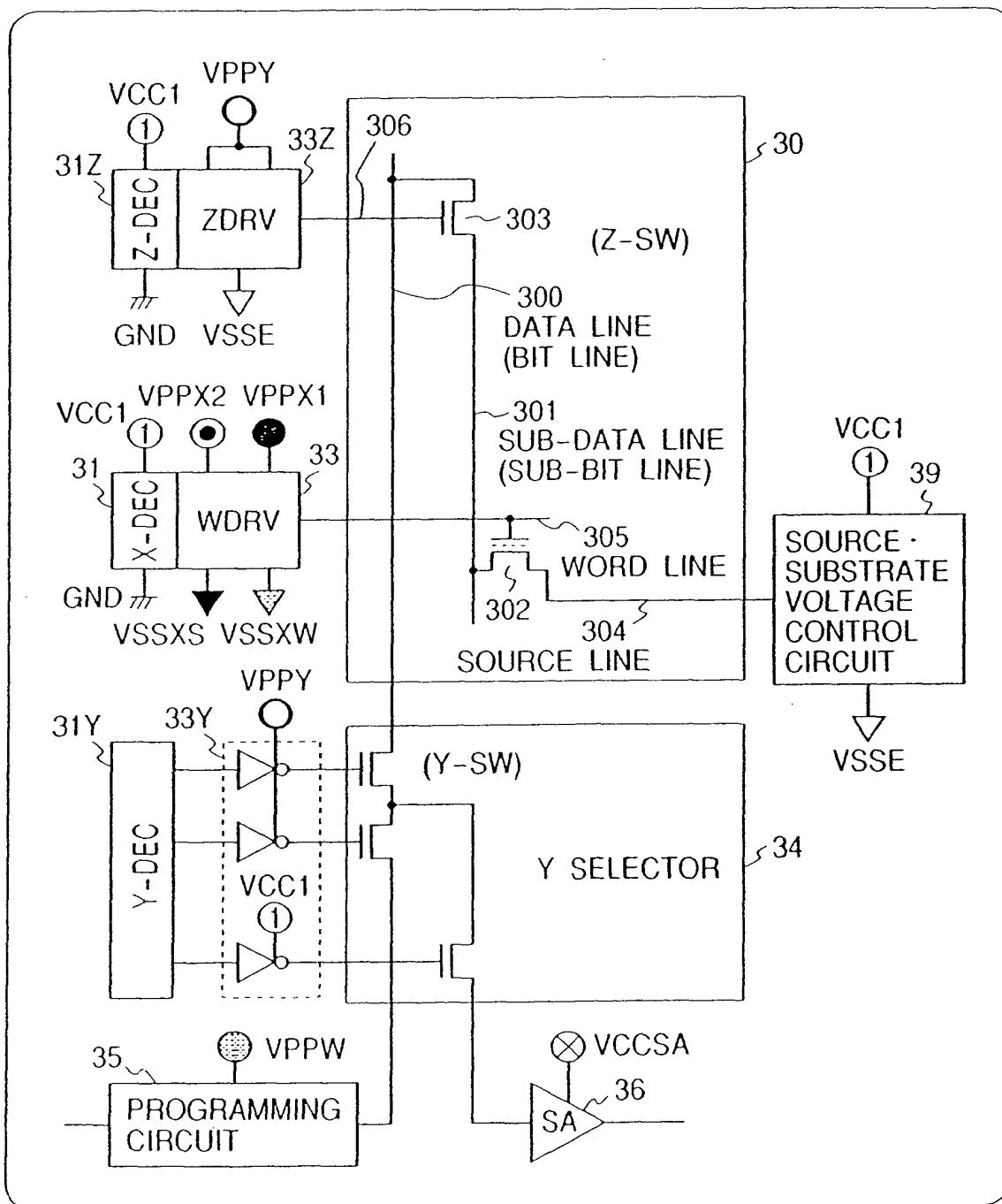


FIG. 9

SYMBOL	NAME	REMARK
○	VCC	Vcc SUPPLY
π	GND	GND SUPPLY
●	VPPX1	POSITIVE VOLTAGE SUPPLY 1 ON WORD DRIVERS
○	VPPX2	POSITIVE VOLTAGE SUPPLY 2 ON WORD DRIVERS
▼	VSSXS	NEGATIVE VOLTAGE SUPPLY FOR SOURCE ON WORD DRIVERS
▽	VSSXW	NEGATIVE VOLTAGE SUPPLY FOR WELL ON WORD DRIVERS
○	VPPY	Y-SW & Z-SW SUPPLY
①	VCC1	LEVEL-SHIFTER SUPPLY
⊗	VCCSA	SENSE AMPLIFIER SUPPLY
●	VPPW	PROGRAMMING CIRCUIT SUPPLY
▽	VSSE	NEGATIVE VOLTAGE SUPPLY FOR CONTROLLING Z-SW, SUBSTRATE AND SOURCE

FIG. 10

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STATE	X-DEC		Y-DEC & Z-DEC		LEVEL-SHIFT	SENSE AMPLIFIER	PROGRAMMING CIRCUIT	Z-SW & SOURCE & SUBSTRATE	
	HIGH	LOW	HIGH	HIGH				HIGH	LOW
VPPX1	VPPX2	VSSXS	VSSXW	VPPY	VCC1	VCCSA	VPPW	VSS	
PROGRAMMING	GND	VfixA (Vstt)	-9.5V (* 2)	-9.5V (* 2)	9.5V (* 1)	VfixA (Vstt)	VfixA (Vstt)	6.5V (* 1)	GND
PROGRAMMING SETUP	Vstt \Rightarrow GND	VfixA (Vstt)	GND \Leftrightarrow -9.5V (BOOSTING)	GND \Leftrightarrow -9.5V (BOOSTING)	Vcc \Leftrightarrow 9.5V (BOOSTING)	VfixA (Vstt)	VfixA (Vstt)	Vcc \Leftrightarrow 6.5V (BOOSTING)	GND
ERASURE	9.5V (* 1)	9.5V (* 1)	GND	GND	VfixA (Vstt)	VfixA (Vstt)	VfixA (Vstt)	VCC	-9.5V (* 2)
ERASURE SETUP	Vcc	Vcc	GND	GND	VfixA (Vstt)	VfixA (Vstt)	VfixA (Vstt)	VCC	-9.5V (* 2)
PROGRAMMING VERIFY	VfixA (Vstt)	VfixA (Vstt)	GND	GND	VfixA (Vstt)	VfixA (Vstt)	VfixA (Vstt)	VCC	GND
ERASE VERIFY	6.5V (* 1)	6.5V (* 1)	GND	GND	VfixA (Vstt)	VfixA (Vstt)	VfixA (Vstt)	VCC	GND
READ	VfixA (Vread)	VfixA (Vread)	GND	GND	Vcc	VfixA (Vread)	Vcc	VCC	GND
	VfixA (Vread)	VfixA (Vread)	GND	GND	Vcc	VfixA (Vread)	Vcc	VCC	GND

*1 : POSITIVE BOOSTING
 *2 : NEGATIVE BOOSTING

FIG. 11

	VPPX1	VPPX2	VSSXS	VSSXW	VPPY	VCC1	VCCSA	VPPW	VSSE
9.5V (*1)	●	●			●				
6.5V (*1)	●	●				●			
Vcc		●	●		●	●			
VfixA			●		●	●			
GND				●	●				
-9.5V (*2)					●				●

*1 : POSITIVE BOOSTING

*2 : NEGATIVE BOOSTING

FIG. 12

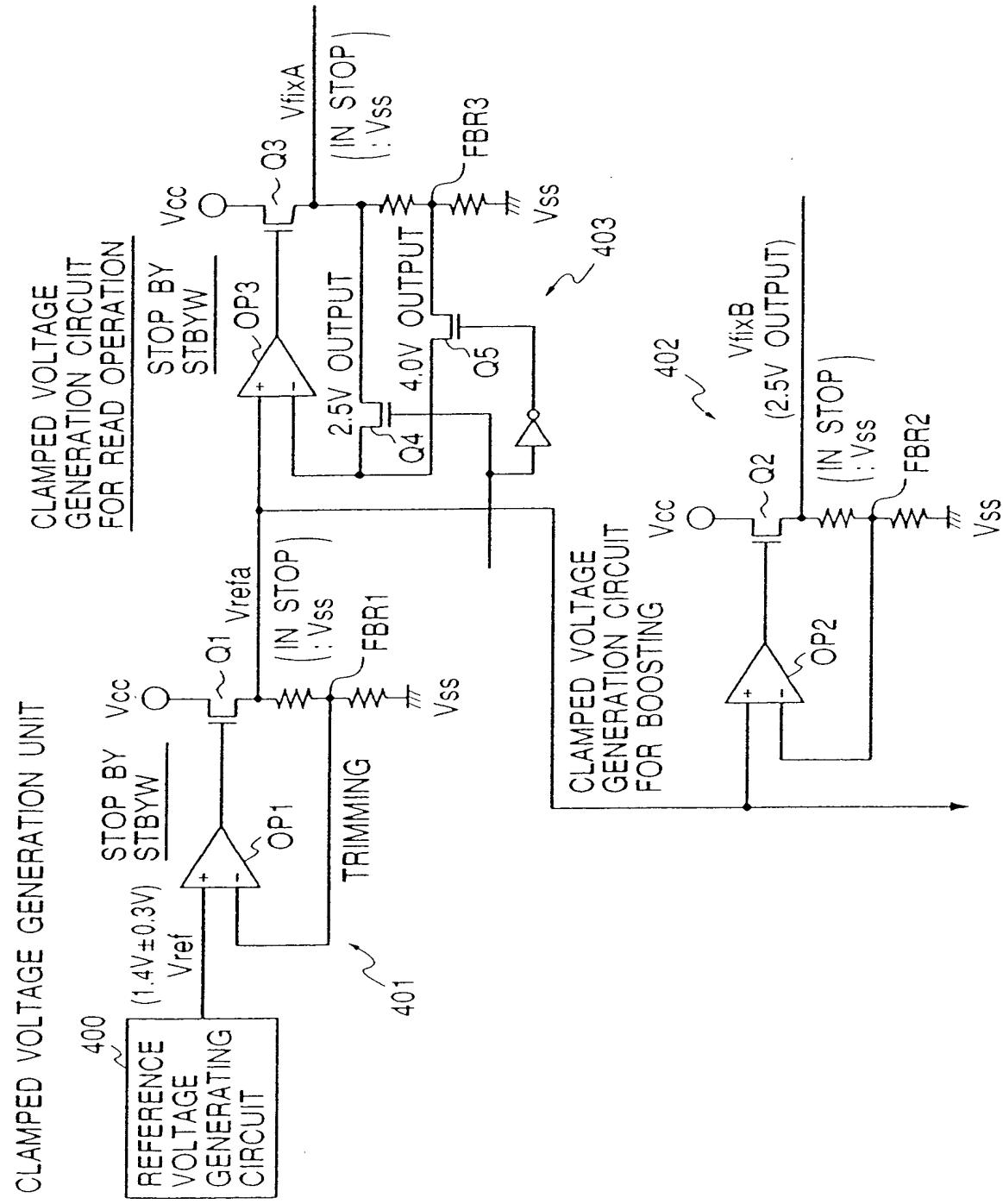


FIG. 13

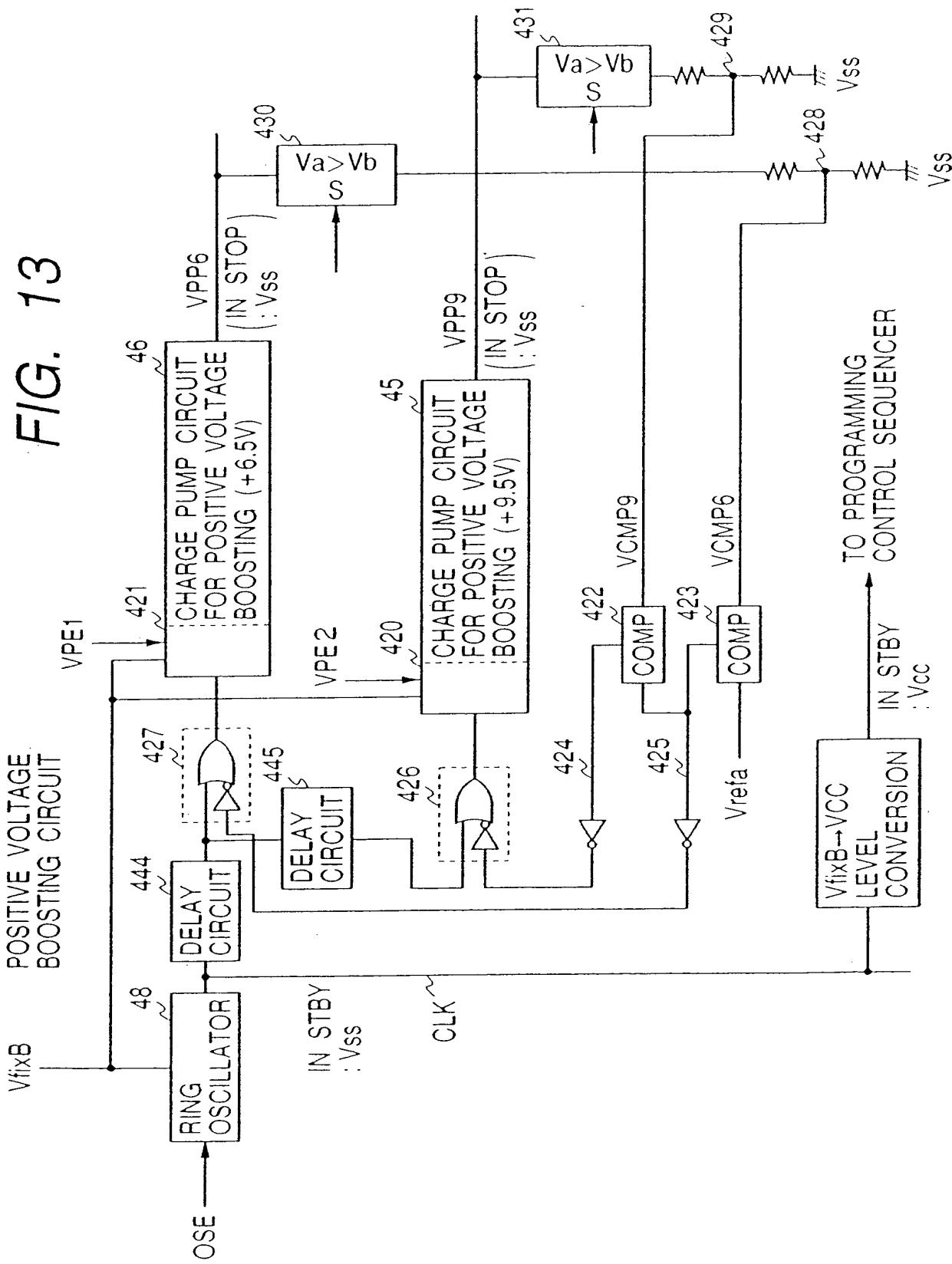


FIG. 14

NEGATIVE VOLTAGE BOOSTING CIRCUIT

CURRENT LOAD EXIST →

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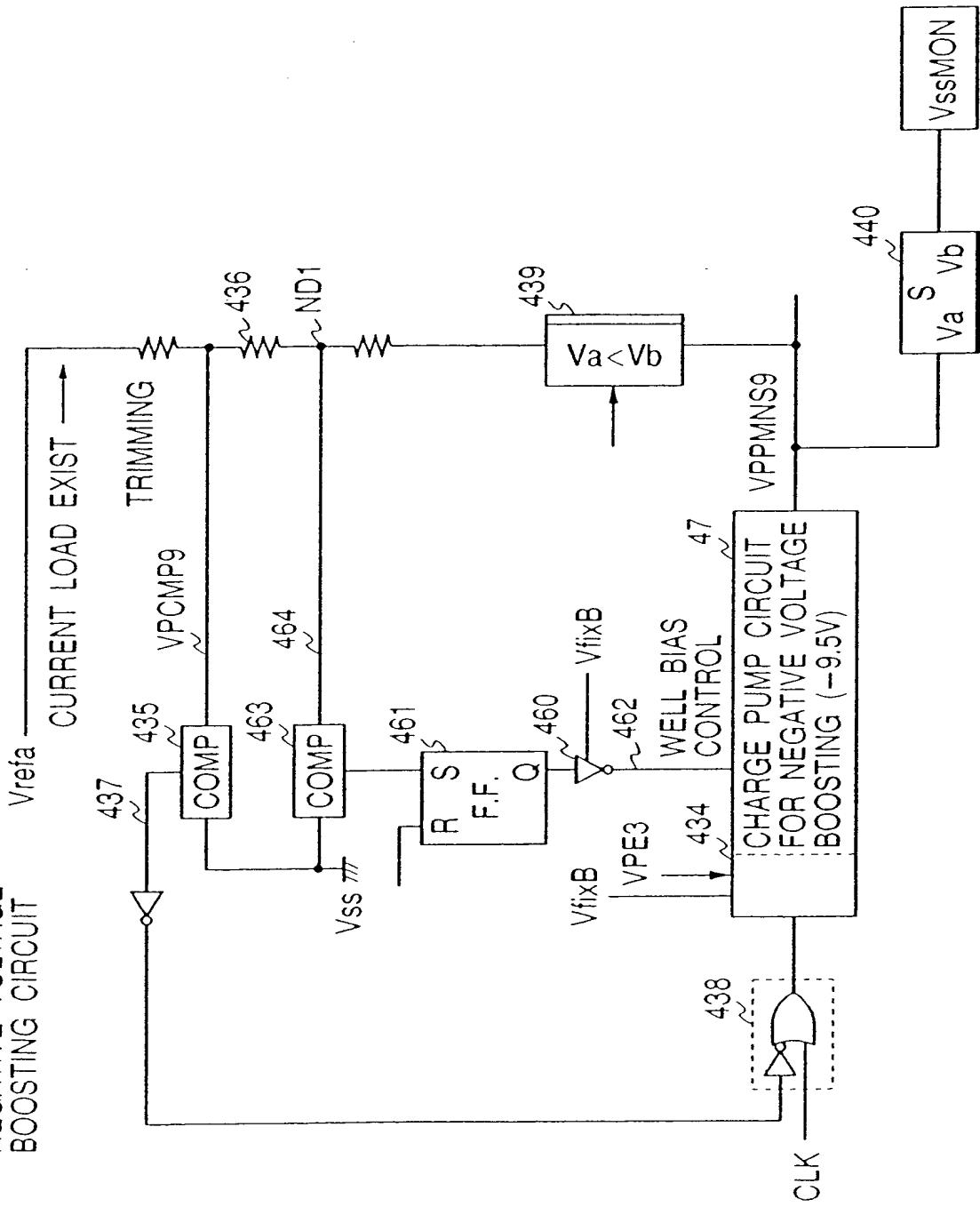


FIG. 15

POSITIVE VOLTAGE MONITOR

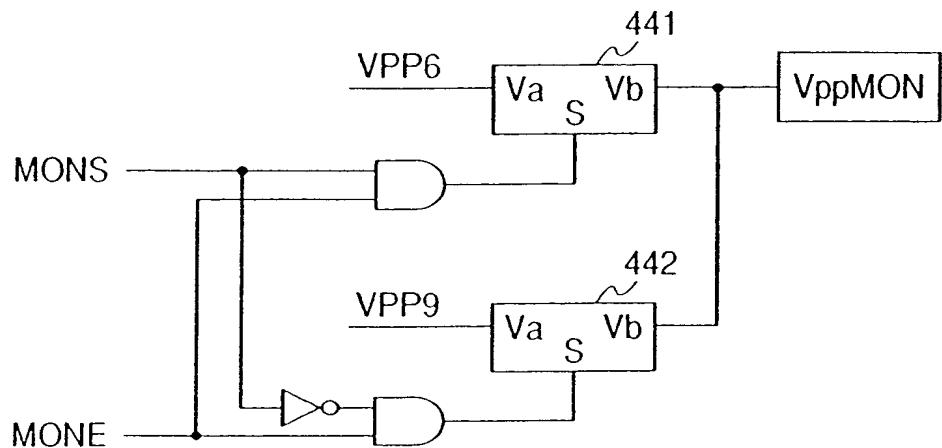


FIG. 16

REFERENCE VOLTAGE TRIMMING

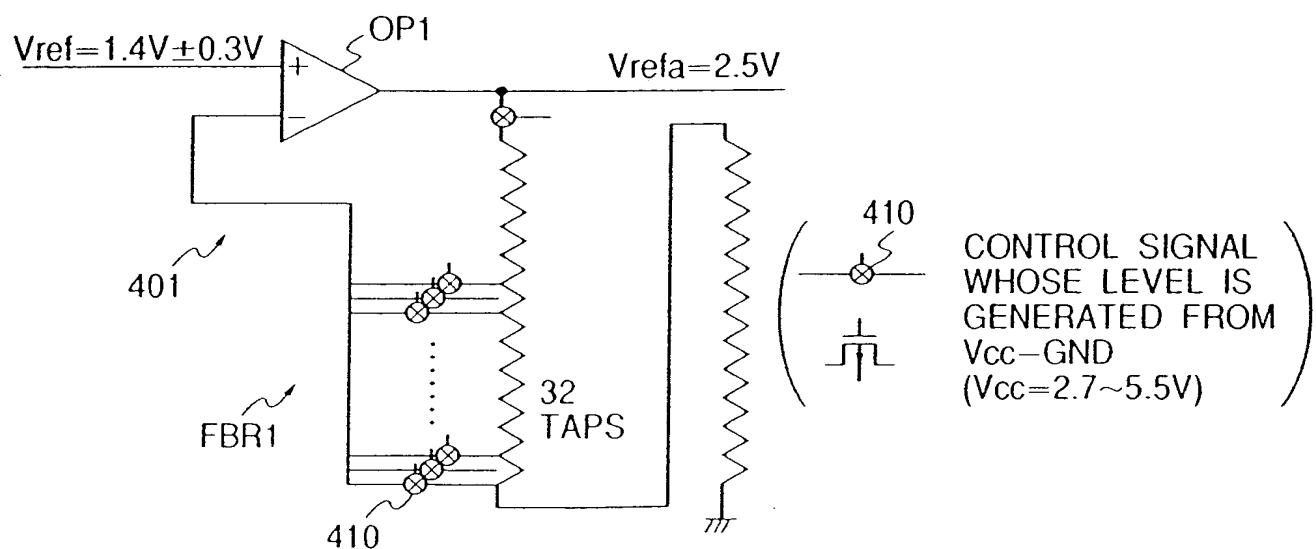


FIG. 17

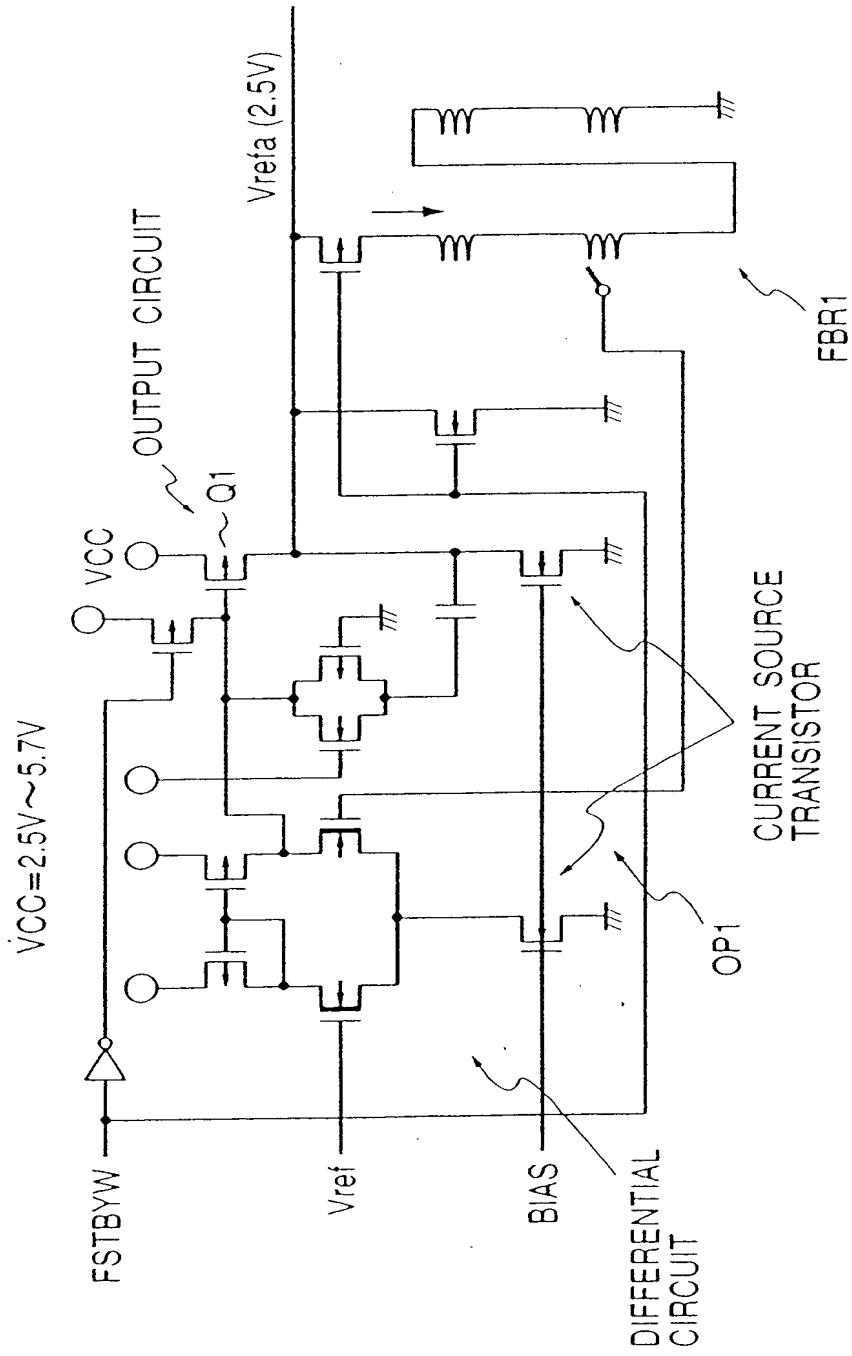


FIG. 18

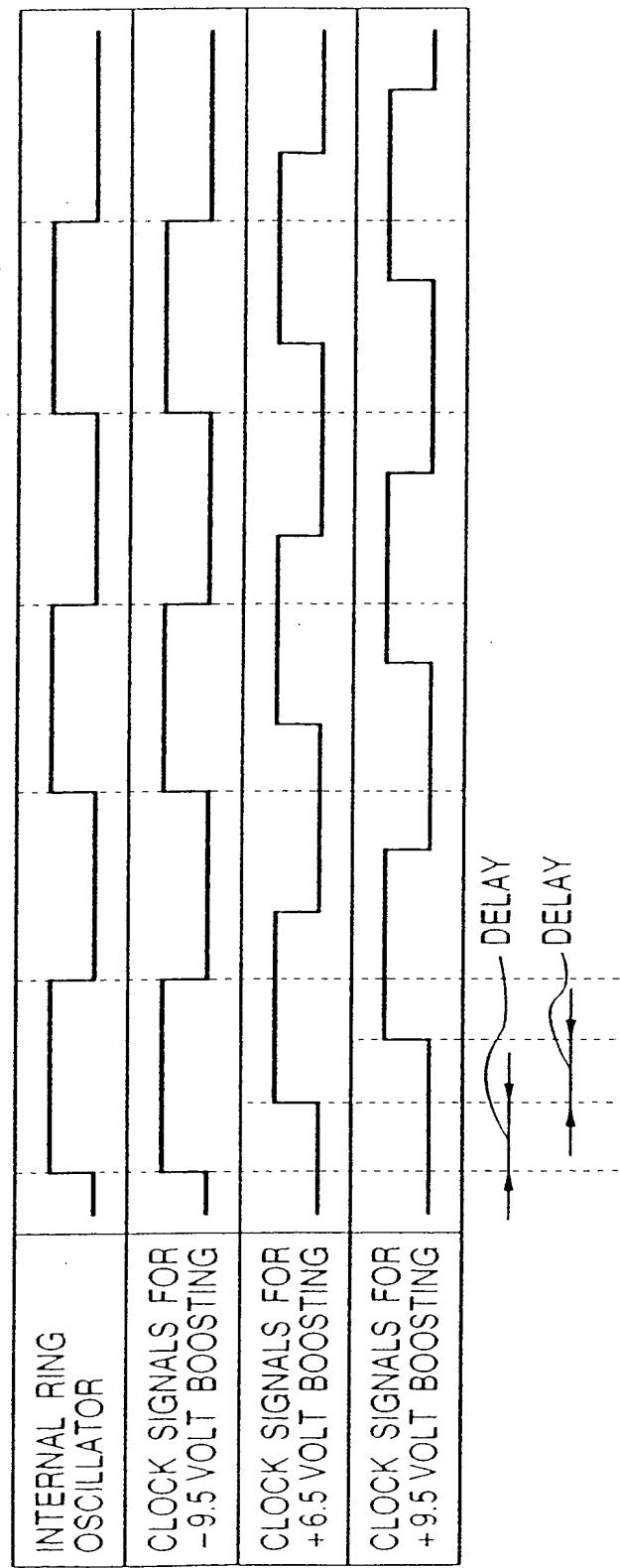


FIG. 19

WELL BIAS ($V_{fixB} - V_{SS}$)

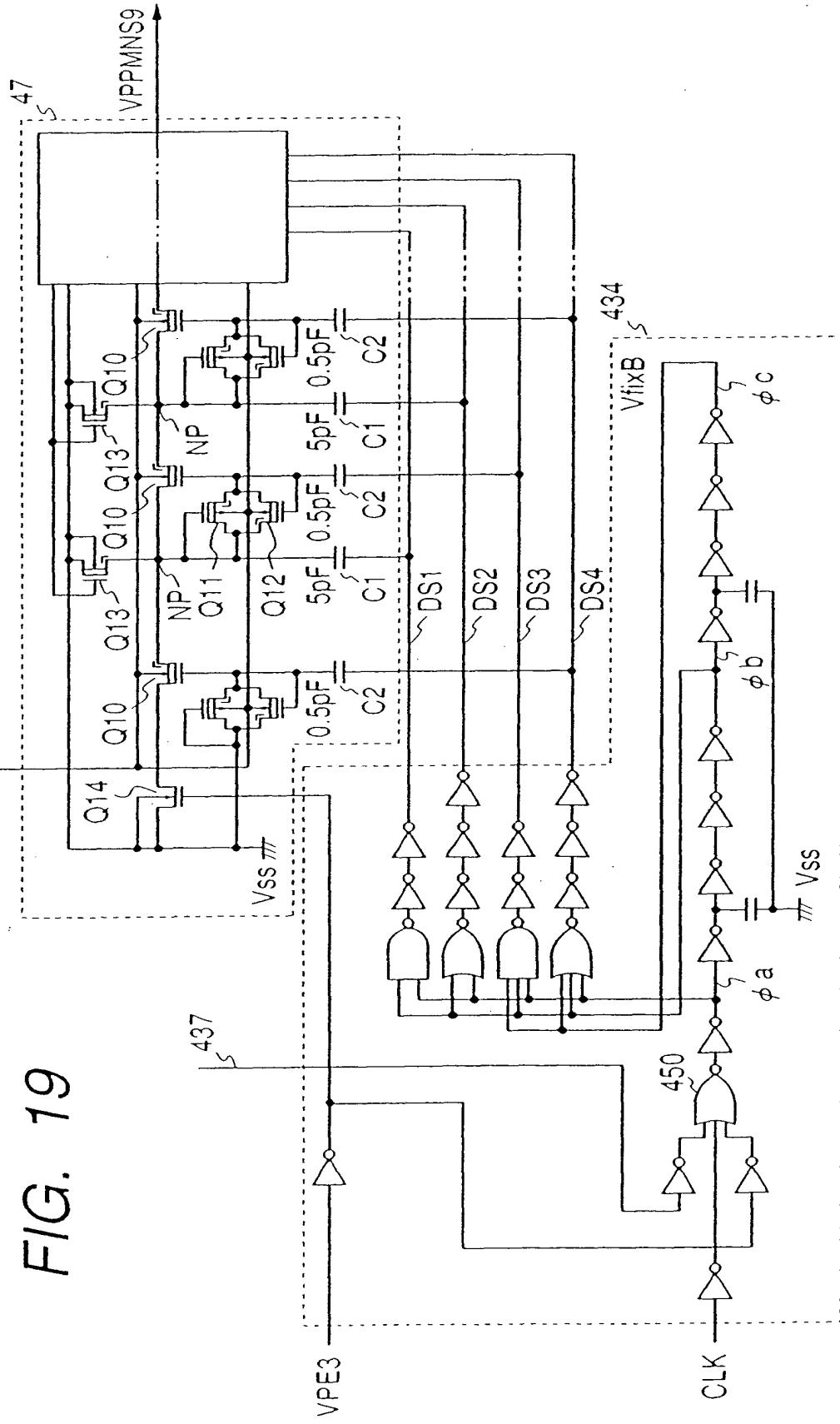


FIG. 20

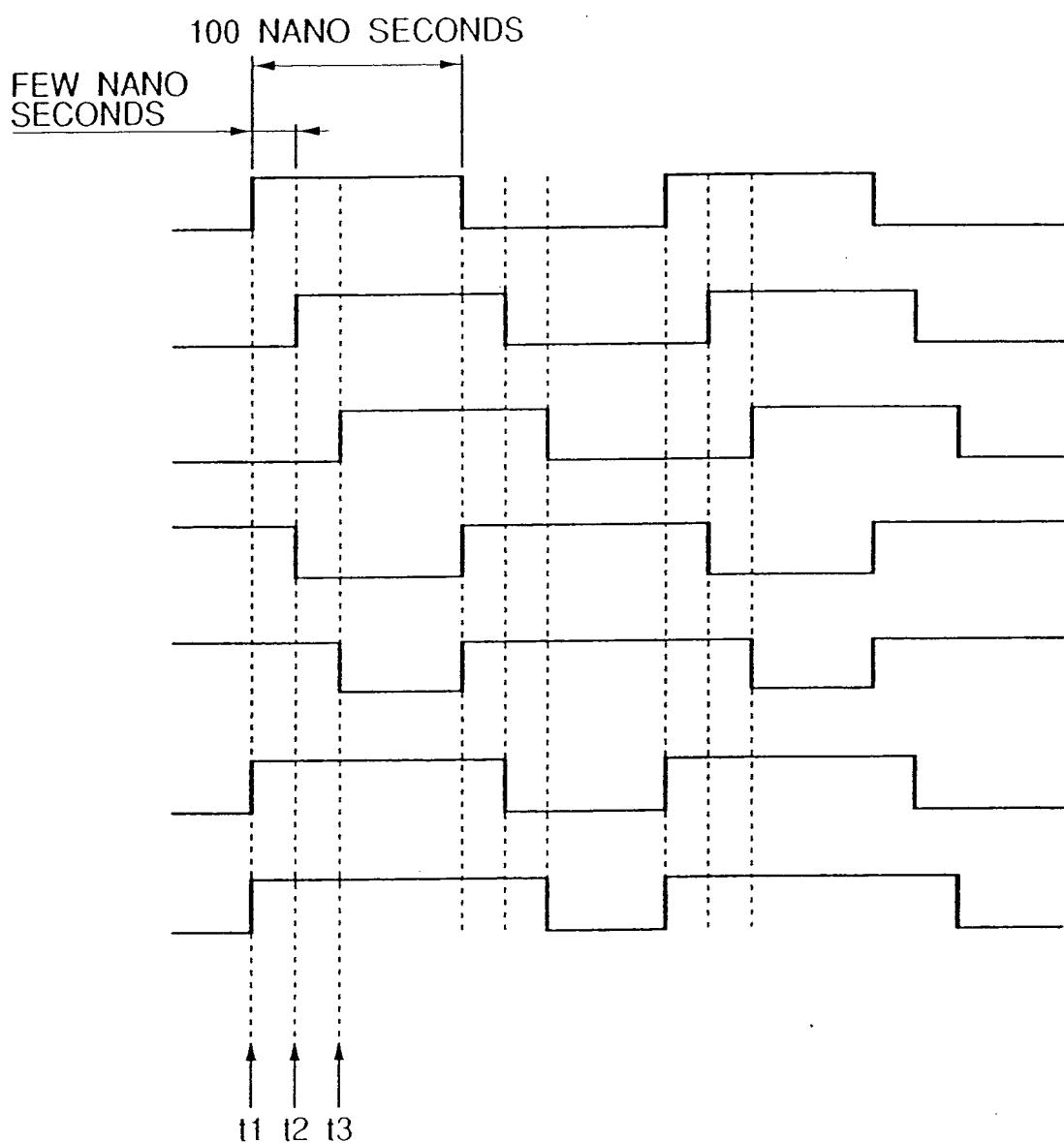


FIG. 21

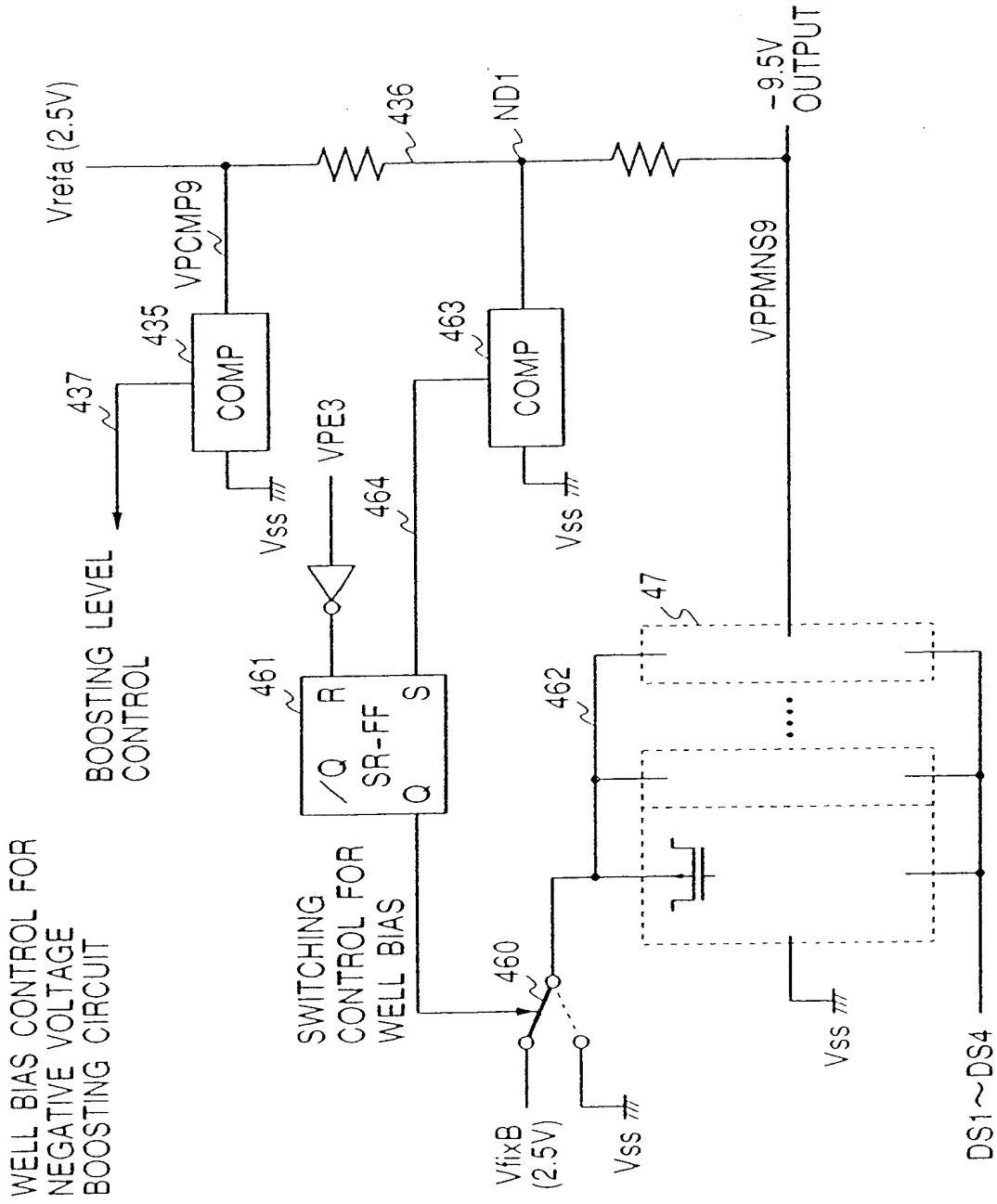


FIG. 22

WELL BIAS CHANGING METHOD FOR NEGATIVE VOLTAGE BOOSTING CIRCUIT

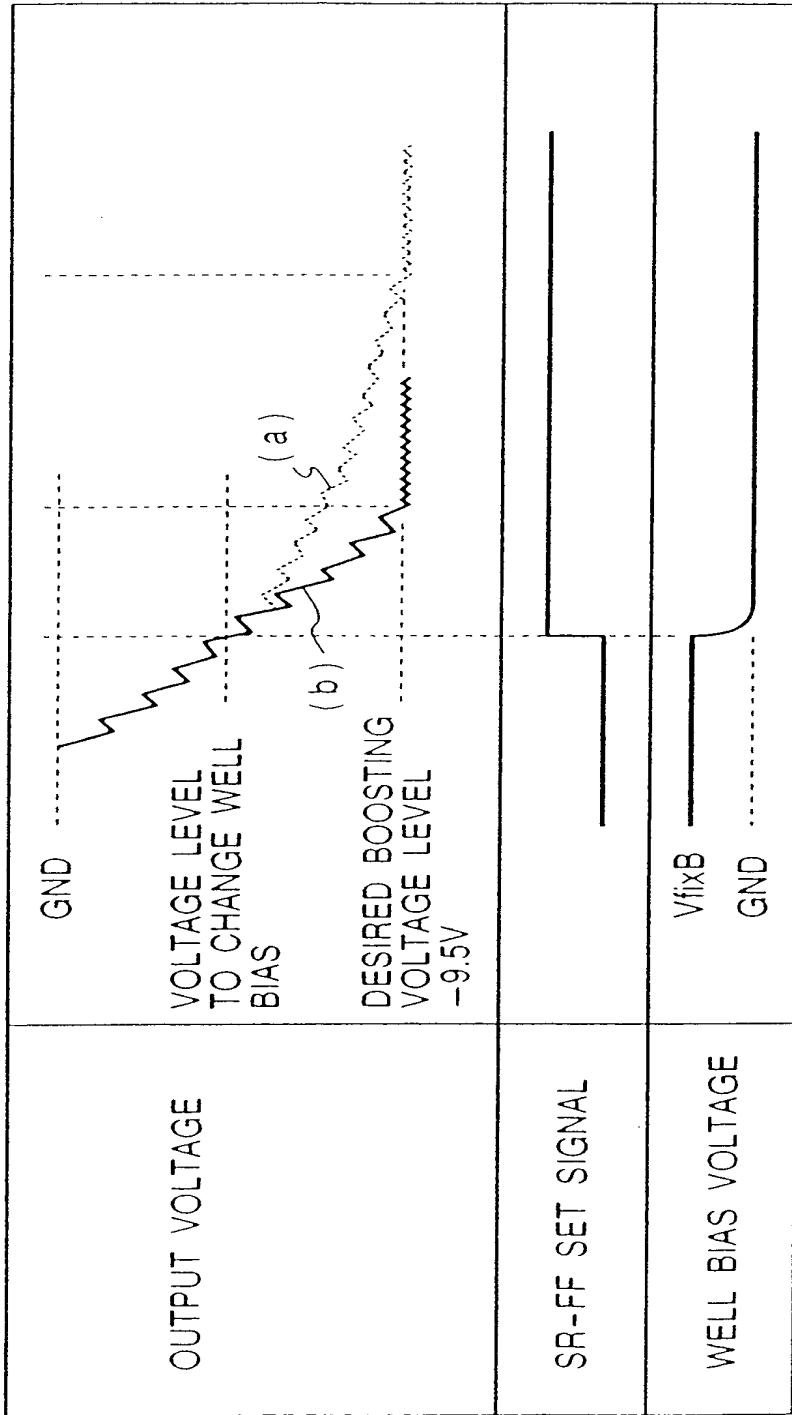


FIG. 23

TRIMMING METHOD

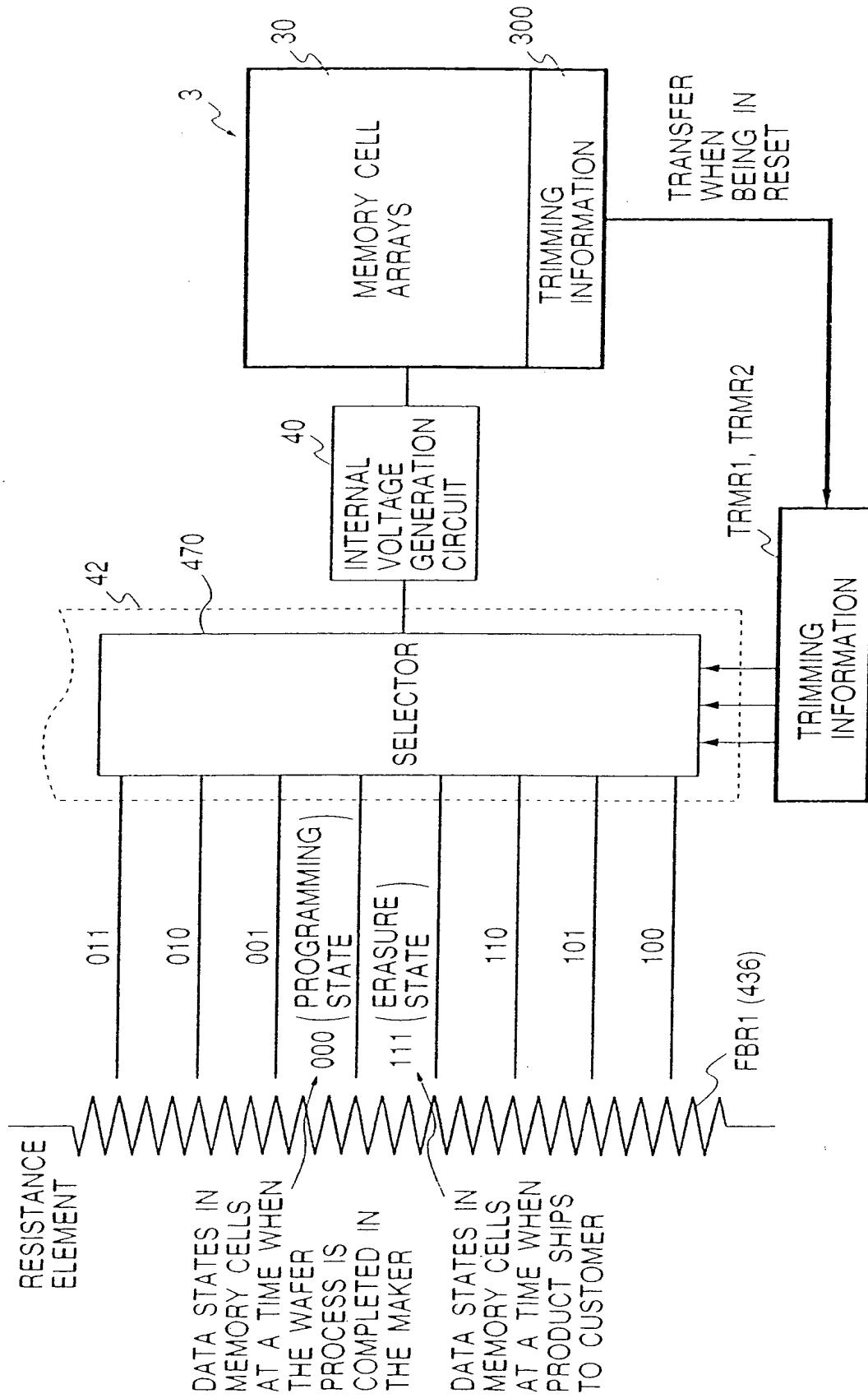


FIG. 24

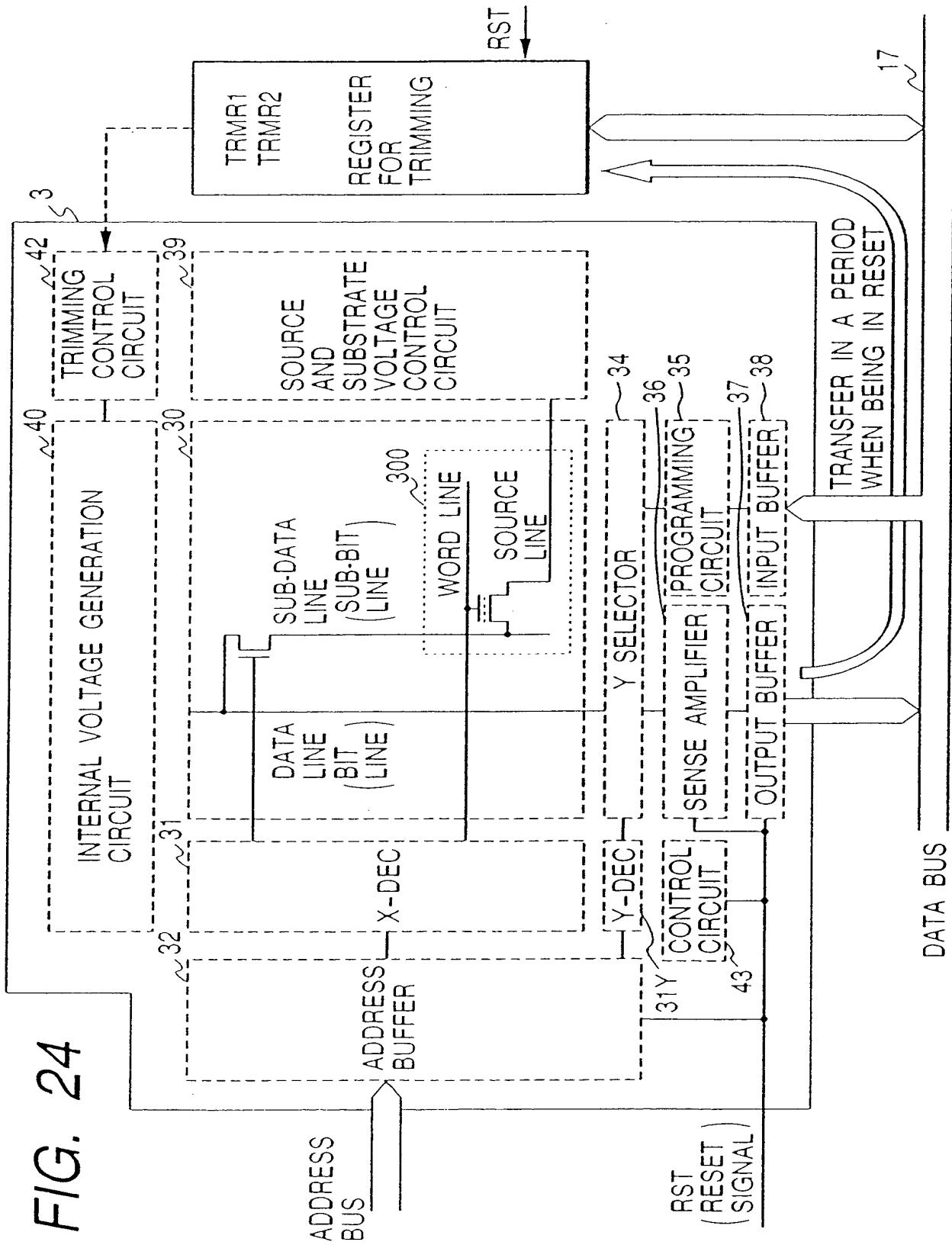


FIG. 25

REGISTER SPECIFICATION
NEW PROVIDED BITS FOR
PROGRAMMING / ERASURE

	A2	A2	A2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
FLMCR1	0	0	0	FWE	SWE	ESU	PSU	EV	PV	E	P
EBR1	0	1	0	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
TRMR1	1	1	0	TEVR	VR4	VR3	VR2	VR1	BR0	—	—
TRMR2	1	1	1	TEVM	VM4	VM3	VM2	VM1	VM0	—	—

FOR TRIMMING

FIG. 26

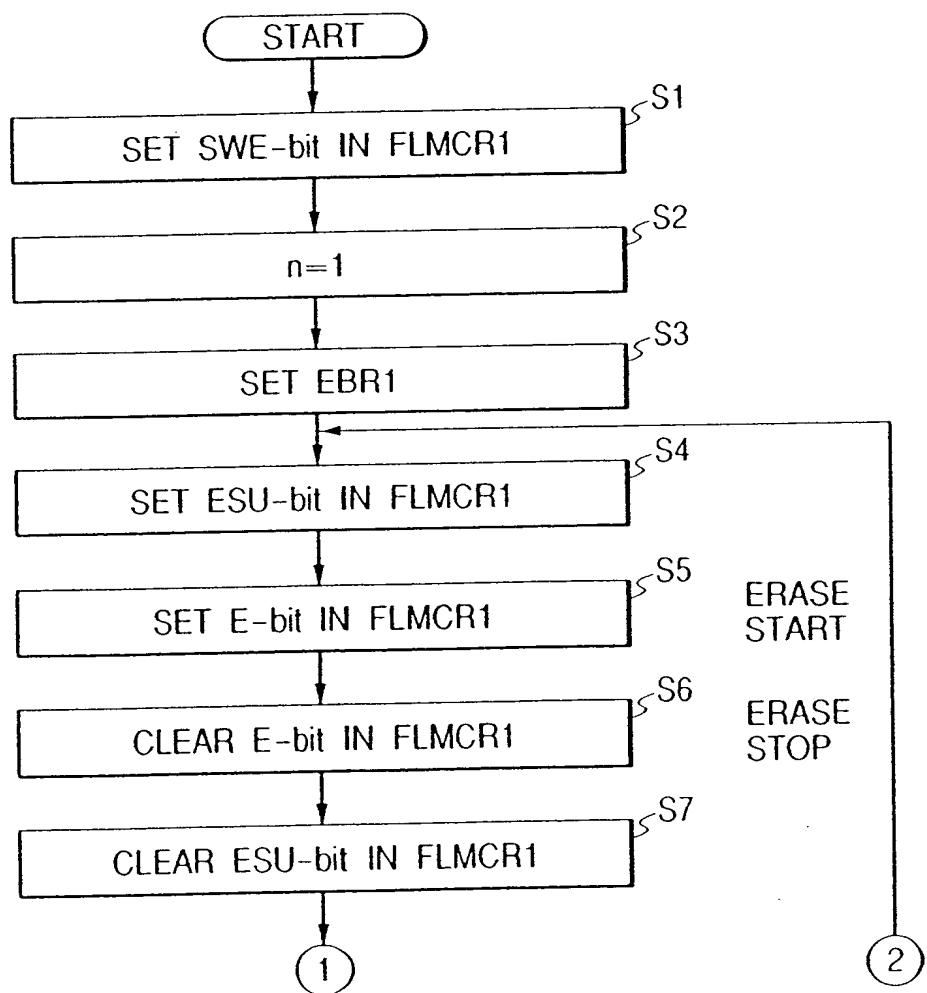
ONE BLOCK ERASURE FLOWCHART

FIG. 27

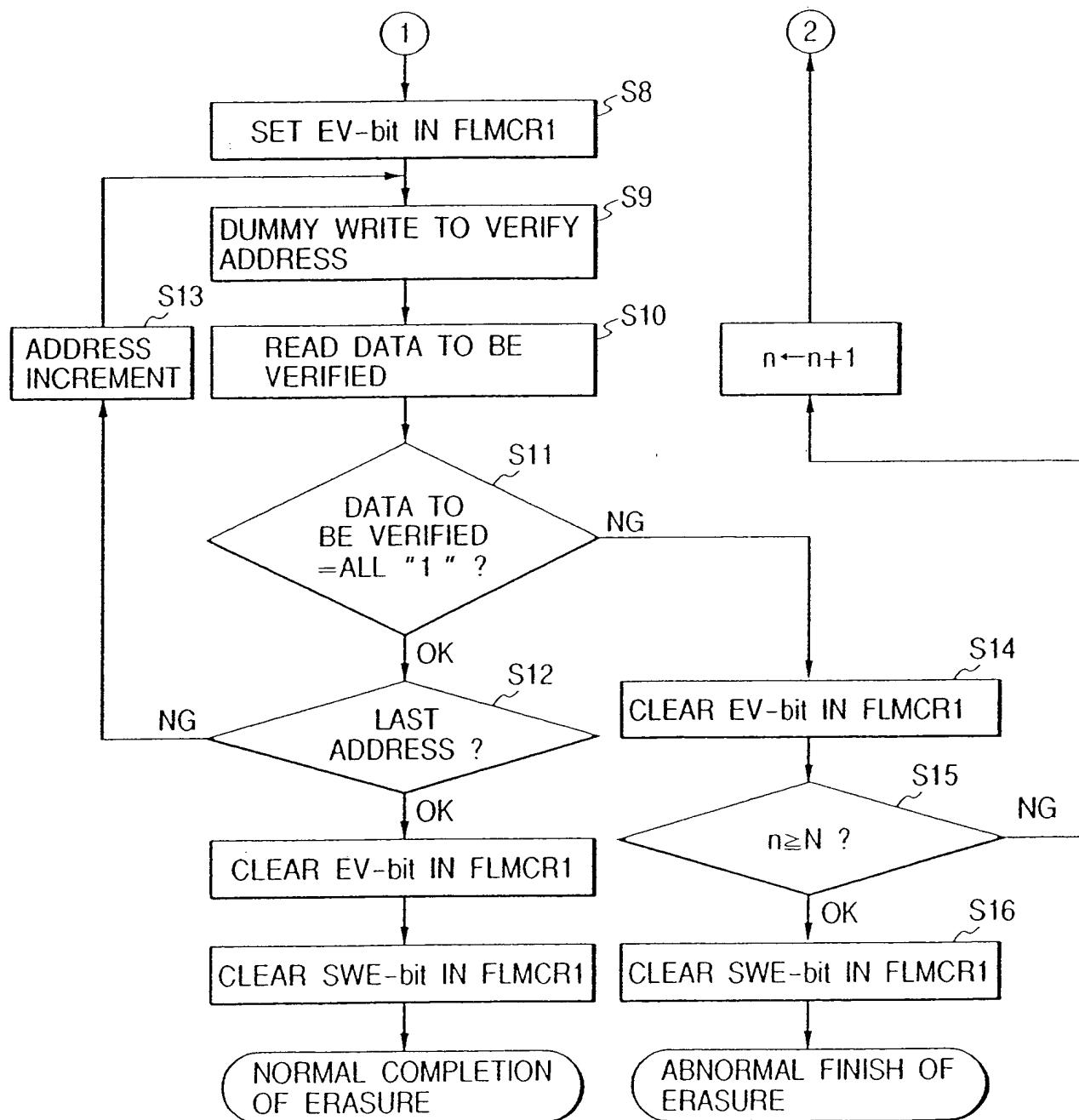


FIG. 28

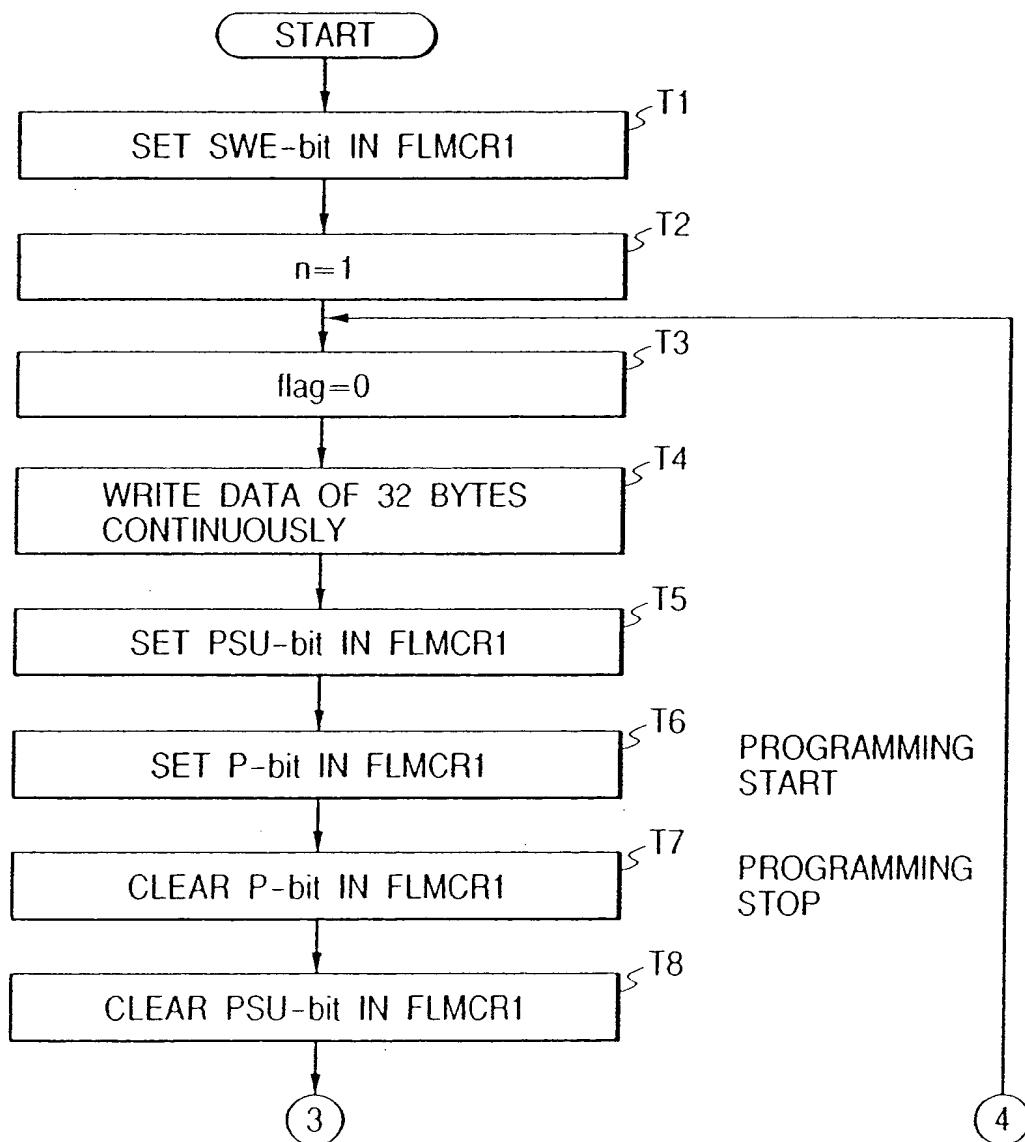
PROGRAMMING FLOWCHART

FIG. 29

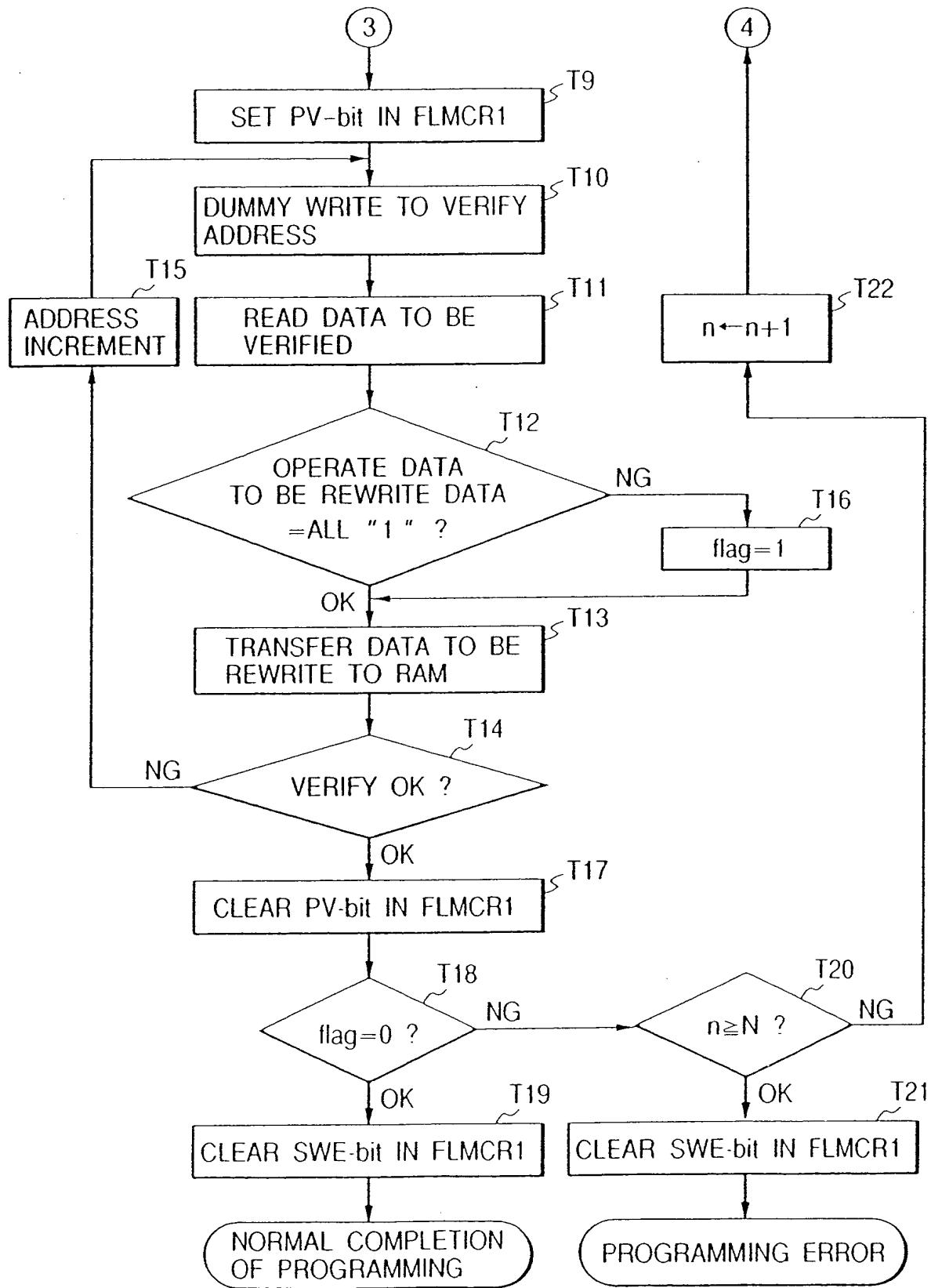


FIG. 30

(*) ERASE STATE OF THE MEMORY CELL IS "1"
 PROGRAMMING IS EXECUTED TO THE MEMORY CELL WHOSE STATE
 IS TO BE DATA "0"

ORIGINAL PROGRAMMING DATA (D)	VERIFY DATA (V)	RE-PROGRAMMING DATA (X)	COMMENT
0	0	1	NO RE-PROGRAMMING IS EXECUTED TO THE MEMORY BIT THAT THE PROGRAMMING HAS BEEN COMPLETED
0	1	0	THE PROGRAMMING IS NOT COMPLETED, RE-PROGRAMMING IS EXECUTED
1	0	1	
1	1	1	ERASE STATE, NO PROGRAMMING IS EXECUTED

FIG. 31

